

INFORMATION DISCLOSURE CITATION  
(Use several sheets if necessary)

Docket Number (Optional)  
13688

Application Number

Applicant(s)  
Richard S. NORMAN et al.

Filing Date  
6-1-01

Group Art Unit

PRO  
U.S. Patent and Trademark Office  
JC920909/870766  
05/01/01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
fr	1.	U.S. 5,008,878	16/04/1991	Ahmadi et al.			
fr	2.	U.S. Re. 34,755	11/10/1994	Eng et al.			
fr	3.	U.S. Re. 34,811	27/12/1994	Eng et al.			
fr	4.	U.S. 5,361,257	01/11/1994	Petersen			
fr	5.	U.S. 5,467,347	14/11/1995	Petersen			
fr	6.	U.S. 5,999,527	07/12/1999	Petersén			
fr	7.	U.S. 5,787,084	28/07/1998	Hoang et al.			
fr	8.	U.S. 5,043,980	27/08/1991	Day, Jr. et al.			
fr	9.	U.S. 6,144,662	07/11/2000	Colmant et al.			
fr	10.	U.S. 5,938,736	17/08/1999	Muller et al.			
fr	11.	U.S. 5,247,513	21/09/1993	Henrion et al.			

FOREIGN PATENT DOCUMENTS

REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Transition	
						YES	NO
12.	EP 0 680 173 A1	02/11/1995	EUROPE				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

fr	13.	Nick McKeown et al. "The Tiny Tera: a Packet Switch Core"; Departments of Electrical Engineering and Computer Science, Stanford University; August 1996; <a href="http://tiny-tera.stanford.edu/tiny-tera/index.html">http://tiny-tera.stanford.edu/tiny-tera/index.html</a>

EXAMINER	fr jay	DATE CONSIDERED
		11/26/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE CITATION</b> <i>(Use several sheets if necessary)</i>				ATTY DOCKET NO.	SERIAL NO.		
				13688-7-2			
				APPLICANT(S)	Richard S. NORMAN et al.		
				FILING DATE	GROUP		
				6-1-01			
<b>U.S. PATENT DOCUMENTS</b>							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JW	14.	U.S. 6,111,856	29/08/2000	Huterer et al.			
JW	15.	U.S. 5,859,835	12/01/1999	Varma et al.			
<b>FOREIGN PATENT DOCUMENTS</b>							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES
							NO
<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>							
EXAMINER				DATE CONSIDERED			

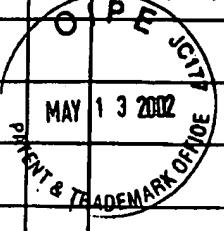
\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		P E AUG 28 2001 JC/SP		Docket Number (Optional) 13688	Application Number 09/870,766	
		PATENT & TRADEMARK OFFICE		Applicant(s) Richard NORMAN et al.	Filing Date June 1, 2001	Group Art Unit 2661
PATENT DOCUMENTS						
EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS
fr	1.	U.S. 4,849,751	18/07/1989	Barber et al.		
fr	2.	U.S. 5,072,366	10/12/1991	Simcoe		
fr	3.	U.S. 4,955,020	04/09/1990	Stone et al.		
RECEIVED AUG 31 2001 Technology Center 2600						
FOREIGN PATENT DOCUMENTS						
REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation
						YES
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)						
fr	4.	French, R., Architectural Consideration for Internet Routers; retrieved from the internet guideline in file; Internet URL <a href="http://www.cise.usf.edu/rfrench">www.cise.usf.edu/rfrench</a> , accessed July 23, 2001;				
fr	5.	Joseph Desposito; Router-On-A-Chip Manages Network Traffic with Wire-Speed QoS; Electronic Design; May 1, 2000; pp 64-65-66;				
EXAMINER <i>fr jyz</i>			DATE CONSIDERED <i>11/26/04</i>			

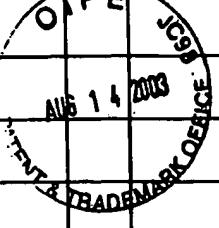
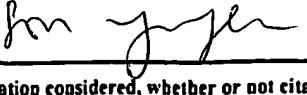
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<b>INFORMATION DISCLOSURE CITATION</b> <i>(Use several sheets if necessary)</i>		Docket Number (Optional) <b>13688</b>	Application Number <b>09/870,766</b>
		Applicant(s) <b>Richard NORMAN et al.</b>	
		Filing Date <b>June 1, 2001</b>	Group Art Unit <b>2661</b>
*EXAMINER INITIAL	<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>		
6.	Werner Bux et al.; Technologies and Building Blocks for Fast Packet Forwarding; IEEE Communications Magazine; January 2001; pp. 70-77. <b>RECEIVED</b> <b>AUG 28 2001</b>		
7.	Minagawa, N. et al. ; Dept. of Comput. Scil, University of Electro-Commun. Tokyo, Japan; Implementation of a network switch on chips; (Abstract) Communications, vol. 13, no. 1; retrieved on March 16, 2001 from INSPEC database. <b>Technology Center</b> <b>AUG 31 2001</b>		
8.	Saturn: a terabit packet switch using dual round-robin; (abstract) Globecom'00 - IEEE, Global Telecommunications Conference; Dept. of Electr. Eng. Polytech, Univ. of Brooklyn, NY, U.S.A.; retrieved on June 4, 2001 from INSPEC database.		
9.	Nanette J. Boden et al.; Myrinet - Gigabit-per-Second Local-Area Network [on line]; November 16, 1994 Myricom, Inc.; Internet URL <a href="http://www.myrinet.com/research/publications/Hot.ps">http://www.myrinet.com/research/publications/Hot.ps</a> ; retrieved on March 14, 2001;		
10.	Vitesse Semiconductor Corporation [on line] ; Datasheet VSC880; January 5, 2001; pp. 1-20; retrieved on July 23, 2001; Internet URL <a href="http://www.vitesse.com/products/documents.cfm.family=180">www.vitesse.com/products/documents.cfm.family=180</a> ;		
11.	Vitesse Semiconductor Corporation [on line] ; Datasheet VSC870; June 29, 2001; pp. 1-40; retrieved July 23, 2001; Internet URL <a href="http://www.vitesse.com">www.vitesse.com</a>		
12.	A New Architecture for Switch and Router Design; PMC-Sierra Inc.; December 22, 1999; Internet URL <a href="http://www.pmc-sierra.com/pressRoom/pht/1cs_wp.pdf">http://www.pmc-sierra.com/pressRoom/pht/1cs_wp.pdf</a> ; retrieved on July 4, 2001; pp. 1-8;		
13.	Network Processor Designs for Next-Generation Networking Equipment [on line] ; EZ Chip Technologies; Internet URL <a href="http://www.ezchip.com/images/pdfs/etchip_white_paper.pdf">http://www.ezchip.com/images/pdfs/etchip_white_paper.pdf</a> ; retrieved on July 4, 2001; December 1999; pp.1-4.		
14.	Cyrel Minkenberg et al. A combined Input and Output Queued Packet-Switched System Based on Prizma Switch-on-a-Chip Technology; Scalable High-Speed Switches/Routers with QoS Support; IBM Research, Zurich Research Laboratory; IEEE Communications Magazine; December 2000; pp 70-84;		
15.	Werner Bux et al.; Technologies and Building Blocks for Fast Packet Forwarding; Telecommunications Networking at the Start of the 21st Century; IEEE Communications Magazine; January 2001; pp 70-77;		
16.	Child, J.; Bus-switching chip busts bandwidth barrier [on line] ; Internet URL <a href="http://www.computer-design.com/editorial/1995/06/directions/bus.html">http://www.computer-design.com/editorial/1995/06/directions/bus.html</a> ; retrieved on March 15, 2001.		
17.	PSID - Based Communications Switching [on line] ; December 1997; Internet URL <a href="http://www.icube.com/commsw.pdf">http://www.icube.com/commsw.pdf</a> ; retrieved on March 15, 2001; pp 1-14		
EXAMINER		DATE CONSIDERED	

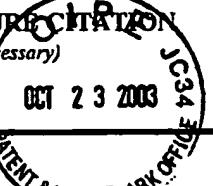
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				Applicant(s) Richard S. Norman et al.			
				Filing Date 06/01/2001	Group Art Unit		
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
S	1.	U.S. 5,377,182	12/27/1994	Monacos			
S	2.	U.S. 5,278,548	01/11/1994	Haber			
 <b>RECEIVED</b> MAY 14 2002 Technology Center 2600							
FOREIGN PATENT DOCUMENTS							
REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
						YES	NO
						YES	NO
						YES	NO
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER		DATE CONSIDERED 11/26/02					

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				Applicant(s) Richard S. NORMAN et al.		Filing Date June 1, 2001	
<b>U.S. PATENT DOCUMENTS</b>							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
				<b>RECEIVED</b> AUG 18 2003 Technology Center 2600			
<b>FOREIGN PATENT DOCUMENTS</b>							
REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
1.	WO 98/26539	06-18-1998	International			YES	NO
2.	EP 1 051 001 A2	11-08-2000	Europe			YES	NO
<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>							
	3.	Partial International Search; PCT/CA02/00810					
EXAMINER				DATE CONSIDERED			
				11/26/04			

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<b>INFORMATION DISCLOSURE STATEMENT</b> <small>(Use several sheets if necessary)</small>				Docket Number (Optional) <b>13688</b>		Application Number <b>09/870,766</b>	
				Applicant(s) <b>Richard S. NORMAN et al.</b>			
				Filing Date <b>June 1, 2001</b>		Group Art Unit <b>2661</b>	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
fr	1.	U.S. 5,790,539	08-04-1998	Chao et al.			
fr	2.	U.S. 5,831,980	11-03-1998	Varma et al.			
	3.	U.S. 6,069,895	05-30-2000	Ayandeh			
<b>RECEIVED</b> OCT 27 2003 Technology Center 2600							
<b>FOREIGN PATENT DOCUMENTS</b>							
REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
4.	EP 0 241 152 A2	10-14-1987	EUROPE			YES	NO
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)							
fr	5.	NOTANI H ET AL: "An 8*8 ATM switch LSI with shared multi-buffer architecture" PROCEEDINGS OF THE SYMPOSIUM ON VLSI CIRCUITS. SEATTLE, JUNE 4-6, 1992, SYMPOSIUM ON VLSI CIRCUITS, NEW YORK, IEEE, US, 4 June 1992 (1992-06-04), pages 74-75, XP010064987					
fr	6.	International Search Report PCT/CA02/00810, August 1, 2003					
<b>EXAMINER</b> <i>fr yng</i>				<b>DATE CONSIDERED</b> <i>11/26/04</i>			

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